ABSTRACT OF THE DISCLOSURE

A SOC processor for multimedia capable of improving three-dimensional graphic process speed includes a pre-processor circuit unit to convert an image signal transmitted from the outside into a compressed input signal for compressing the image signal, an encoder/decoder circuit unit to create a compressed data by compressing the compressed input signal, and to encode the compressed data, a post-processor to convert the coded image signal so that an image displaying apparatus can use the image signal, a graphic accelerator to process three-dimensional graphic computation with respect to the image signal output on the image displaying apparatus, a first system bus connected with the encoder/decoder circuit unit, a second system bus connected with the pre-processor, post-processor, and graphic accelerator, and a controlling unit to control the above circuit units. The first system bus and second system bus can communicate data each other by a bridge DMA circuit unit.